Department of Electrical Engineering and Computer Science
ECE 351 Digital Systems Design, Spring 2014

Course Objectives:
This course introduces the challenges, methodologies, techniques, and issues for designing digital systems, in particular, based on reprogrammable FPGA devices. These devices could be easily reconfigured via VHDL programming and realize heterogeneous types of digital system functionalities. The recommended background of this course is basic understanding of computer architecture, computational logic, and computer programming. There will be programming assignments and hardware/software co-design projects in this course, so hands-on skills on system developments are also required.

Upon completion of this course, every student should have gained:
1. An understanding of the generic design, analysis, and implementation methodology of digital systems.
2. A broad familiarity of the system-level FPGA operations and designs on both hardware and software aspects.
3. A basic mastery of VHDL programming skills, and the hands-on skills about applying the VHDL-reconfigurable FPGA devices over multiple digital system components, such as mice, displays, keyboards, etc. The students will also gain experiences of developing realistic digital system applications by integrating various system components together.

Instructor:
Dr. Wei Gao
Office: 302 Min Kao, Email: weigao@utk.edu, Phone: 865-974-3984
Office Hour: TR 11:00am – 12:00pm or by appointment, 302 Min Kao

Class/Laboratory Schedule:
Class: TR 9:40am – 10:55am, 405 Min Kao
Laboratory: TBD

Textbooks and/or Other Required Material:
Textbook:
The Designer's Guide to VHDL. Peter J. Ashenden, 3rd edition, Morgan Kaufmann, 2008.

References:
The Student's Guide to VHDL. Peter J. Ashenden, 2nd edition, Morgan Kaufmann, 2008.

Digital Design: An Embedded Systems Approach Using VHDL, Peter J. Ashenden, Morgan Kaufmann, 2008.

FPGA-Based System Design, Wayne Wolf, Prentice Hall, 2004.

Topics Covered:
Digital system design concepts
Combinatorial and sequential logic design: principles and practices
Sequential and combinatorial VHDL design
Synchronous and asynchronous design
Testbench development
FPGA timing analysis
FPGA power analysis
CAD design software and emulation testbed
Applications of FPGA in practical digital system development
Cyber-physical systems

Grading Policy:
Labs (3): 15%
Course project: 40%: proposal: 5%, midterm presentation: 10%, final presentation: 10%, final report 15%.
Midterm exam: 15%
Final Exam: 25%
Participation: 5%

Academic Integrity:
All programs turned in for credit must be each student's own work. Students **must** write their own programs and problem solutions from scratch independently. **No collaboration** is allowed for lab assignments. **Closed-book** exams. **No discussion** is allowed during exams. Any violations will result in a ***minimum penalty of a zero*** on the given assignment or exam.

Disability Statement:
Any student who feels s/he may need an accommodation based on the impact of a disability should contact the Office of Disability Services at 865-974-6087 in Hoskins Library to coordinate reasonable accommodations for students with documented disabilities.