

FPGA implementation of 0-99
Cyclic code decade counter

LAB #2 EE 2160
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Purpose:

To implement the schematic of the 8bit 0-99 counter on the Excalibur target board, with on board FLEX20K200EFC484-2X FPGA chip and in the process learn pin assignments procedure. The final goal is to display the output on the on-board 7-segment LED display.

Procedure:

In order to properly display the count from 0-99 on the seven segment LED displays, the output from lab 1 was converted from the BCD sequence 0, 1, 3, 2, 6, 14.... to the sequence 0, 1, 2, 3, 4, 5, 6, To achieve this, a VHDL code converter logic block was developed using the VHDL code from the given lab assignment. The input to this code converter logic block was the output from the decade counter.

The next step was to connect the output from the code converter to the seven segment displays. For this, a 74247 decoder was used. Each of the decade counters was connected to its own 74247 decoder.

The next step was to modify the 33.3 MHz clock signal from the Excalibur board. The clock signal needs to be modified since it will update the counters too quickly for the human eye to detect. For this the signal was converted to a 2 Hz signal. At this rate, the seven segment display will update twice every 1 second. In order to implement this, a 24 bit counter was implemented. Using the “MegaWizard Plug-In Manager”, a 24 bit counter logic block was generated. Using the following calculations, the 24th bit was chosen to obtain a 2 Hz clock frequency:

$$33.3 \text{ MHz} / (2^{24}) = 2 \text{ Hz}$$

The 24th bit output from the counter was then used as input to the clock signal on the DFF.

The next step was to assign input and output pins from the Quartus design to the Excalibur board. For this, the Excalibur Pin Assignments datasheet was used. The seven output pins from each 74247 BCD were mapped to the seven segment displays on the Excalibur board. The clock signal was mapped to pin L6 and the reset signal was mapped to the push button SW4. Please see the design section of this lab report for a complete list of the pin assignments.

The final step was to download the compiled design on the Excalibur board. The JTAG cable was connected from the parallel port of the computer to the JP3 terminal on the board. The power adapter was connected from the board to the power supply. After giving the “start programming” command on the Quartus menu, the results were seen on the 7 segment LED displays.

Design:

Creation of the CodeConverter.vhd:

The VHDL code to convert the cyclic code count to a 0-9 binary count is a simple case statement that maps every cyclic code to its equivalent binary output. The symbol thus created is used in the schematics between the decade counter and the 74247 decoder, which expects a binary increment to display 0-9 on the seven segment LED.

```
*****
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

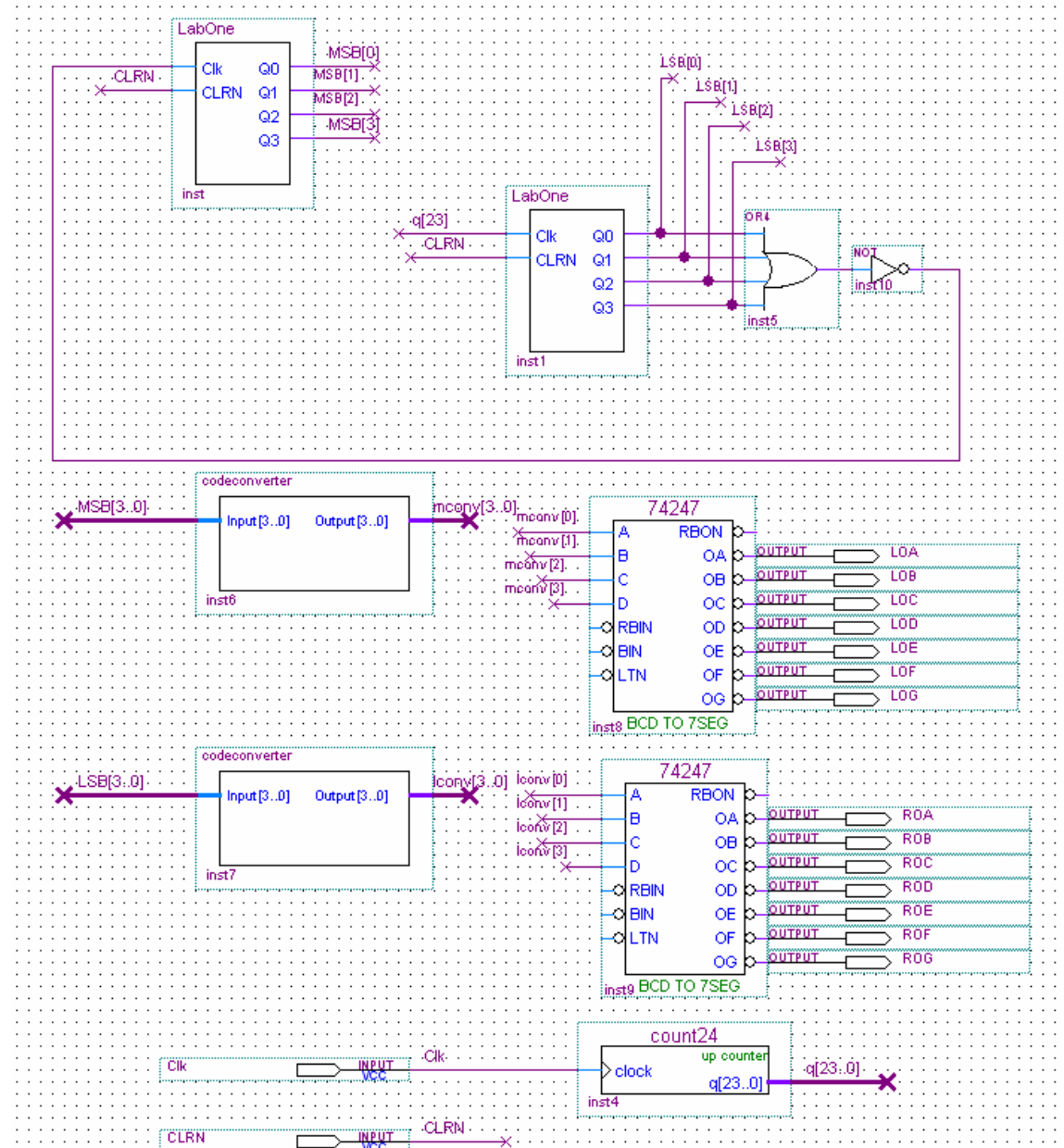
ENTITY CodeConverter IS
    PORT(
        Input      : IN    std_logic_vector(3 DOWNTO 0);
        Output     : OUT   std_logic_vector(3 DOWNTO 0)
    );
END CodeConverter;

ARCHITECTURE dataflow OF CodeConverter IS
BEGIN
    Output <=
        "0000" when Input = "0000" else
        "0001" when Input = "0001" else
        "0010" when Input = "0101" else
        "0011" when Input = "0111" else
        "0100" when Input = "0110" else
        "0101" when Input = "1110" else
        "0110" when Input = "1100" else
        "0111" when Input = "1101" else
        "1000" when Input = "1001" else
        "1001" when Input = "1000" else
        "1110"; -- "1110" signifies an error condition
END dataflow;
*****
```

The lab1 design was modified to include the Cyclic to Binary converter, 74247 decoder, and the step down clock 24 bit up counter. The schematic shown in Figure1 gives the interconnection of the various elements.

Note: A-D of 74247 decoder maps to [0-3] of the 4 bit counter

Figure 1: Schematic of FPGA implementation of 0-99 Counter



The pin assignment procedure is the process of mapping the logical pins of the schematic to the physical wires on the Excalibur target board. The Pin mapping from the reference excel sheet used for this lab are :

Excalibur Pin Assignments (External I/O)

Seven Segment Left		Seven Segment Right		Push Buttons	
Name	APEX Pin	Name	APEX Pin	Name	APEX Pin
a	R11	a	R10	SW7	W9
b	U11	b	T11	SW6	Y8
c	Y7	c	U8	SW5	T9
d	V8	d	W18	SW4	Y9
e	Y17	e	Y18	Clock	
f	V18	f	U18	Name	APEX Pin
g	V17	g	W17	Clock	L6

The left seven segment pins LOA-LOG maps to R11, U11,Y7, V8,Y17,V18,V17, the left segment, displays the most significant nibble of the 8 bit counter. The right segment pins ROA-ROG maps to R10, T11, U8, W18, Y18, U18, W17, the right segment, displays the least significant nibble of the 8 bit counter. (See Figure 2).

Figure 2: Table of Pin Assignments

	Source Name (From)	Destination Name (To)	Option	Value
1		CLRN	I/O Standard	LVTTL
2		Clk	I/O Standard	LVTTL
3		LOA	I/O Standard	LVTTL
4		LOB	I/O Standard	LVTTL
5		LOC	I/O Standard	LVTTL
6		LOD	I/O Standard	LVTTL
7		LOE	I/O Standard	LVTTL
8		LOF	I/O Standard	LVTTL
9		LOG	I/O Standard	LVTTL
10		ROA	I/O Standard	LVTTL
11		ROB	I/O Standard	LVTTL
12		ROC	I/O Standard	LVTTL
13		ROD	I/O Standard	LVTTL
14		ROE	I/O Standard	LVTTL
15		ROF	I/O Standard	LVTTL
16		ROG	I/O Standard	LVTTL
17		CLRN	Location	Pin_Y9
18		Clk	Location	Pin_L6
19		LOA	Location	Pin_R11
20		LOB	Location	Pin_U11
21		LOC	Location	Pin_Y7
22		LOD	Location	Pin_V8
23		LOE	Location	Pin_Y17
24		LOF	Location	Pin_V18
25		LOG	Location	Pin_V17
26		ROA	Location	Pin_R10
27		ROB	Location	Pin_T11
28		ROC	Location	Pin_U8
29		ROD	Location	Pin_W18
30		ROE	Location	Pin_Y18
31		ROF	Location	Pin_U18
32		ROG	Location	Pin_W17

Note: The pin type 'LVTTL' is chosen for all pin assignments, and all unconnected inputs tristated. The Clk was assigned to L6 and CLRN – the clear to the flip-flops was assigned to the SW4 –(push button).

Results

The seven segment LED display, counted 0-99 and looped over, thus validating our design. The clock input was changed from 2hz to higher speeds to see a faster counter implementation. Higher clock speeds obtained by tapping not the 24th bit but lower order bits (for instance the 20th bit would give a clock of $33.3 \text{ MHz} / (2^{20}) = 32 \text{ Hz}$).

Both the TFF and DFF implementations of the decade counter were programmed in FPGA and – the 0-99 count display on the seven segment LED was verified.

Conclusion

The cyclic code decade counter that was designed using flip-flops and logic gates in lab1 was tested on the Altera Excalibur FPGA target board. The seven segment LED display was used to verify the 0-99 count, of the cascaded 4 bit cyclic decade counter.

This assignment was very useful in teaching us about pin-assignments (mapping between the logical nodes of the schematic to the physical nodes on the target board) and to program the target board using the JTAG cable.