Introduction to
CMOS VLSI
Design

Lecture 4:
CMOS Transistor Theory

David Harris, Harvey Mudd College
Kartik Mohanram and Steven Levitan
University of Pittsburgh
Outline

- Introduction
- MOS Capacitor
- nMOS I-V Characteristics
- pMOS I-V Characteristics
- Gate and Diffusion Capacitance
- Pass Transistors
- RC Delay Models
Introduction

- So far, we have treated transistors as ideal switches
- An ON transistor passes a finite amount of current
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitance
  - $I = C \left(\frac{\Delta V}{\Delta t}\right) \Rightarrow \Delta t = \frac{C}{I} \Delta V$
  - Capacitance and current determine speed
- Also explore what a “degraded level” really means
MOS Transistors - Types and Symbols

NMOS Enhancement  NMOS Depletion

PMOS Enhancement  NMOS with Bulk Contact

© Digital Integrated Circuits 2nd Devices
The MOS Transistor
Controlling current flow in an nFET.

(a) Zero gate voltage

(b) Positive gate voltage
Controlling current flow in a pFET.

(a) High gate voltage

V_G negative

(b) Negative gate voltage

Open switch

Closed switch

Hole channel
What is a Transistor?

A Switch! \[ V_{GS} \geq V_T \]  \[ \rightarrow \]  A MOS Transistor

|V_{GS}|
I-V Curves

Current (I) vs. Voltage (V)

I = f(V)

Resistor
I = V/R

Diode
I = I_s \cdot \exp(k \cdot V - V_t)

MOS
I = f(V_{gs}, V_{ds})
Terminal Voltages

- Mode of operation depends on $V_g$, $V_d$, $V_s$
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$

- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$

- nMOS body is grounded. First assume source is 0 too.

- Three regions of operation
  - Cutoff
  - Linear
  - Saturation
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion

In general, MOS gate capacitance is not constant
MOS Transistors – Operating regions

(a) Cutoff: No Channel
\[ I_{ds} = 0 \]

(b) Linear: Channel Formed
\[ I_{ds} \text{ Increases with } V_{ds} \]

(c) 0 < \( V_{ds} < V_{gs} - V_{t} \)

(d) Saturation: Channel Pinched Off
\[ I_{ds} \text{ Independent of } V_{ds} \]

**FIG 2.3** nMOS transistor demonstrating cutoff, linear, and saturation regions of operation

Copyright © 2005 Pearson Addison-Wesley. All rights reserved.
nMOS Cutoff

- No channel
- \( I_{ds} = 0 \)
nMOS Linear

- Channel forms
- Current flows from d to s
  - $e^-$ from s to d
- $I_{ds}$ increases with $V_{ds}$
- Similar to linear resistor

$$I_{ds} \text{ increases with } V_{ds}$$
Linear Region $V_{gs} > V_t$ & $V_{gd} > V_t$

Positive Charge on Gate:
Channel exists, Current Flows since $V_{ds} > 0$

$$I_{ds} = k'(W/L)((V_{gs}-V_t)V_{ds}-V_{ds}^2/2)$$
nMOS Saturation

- Channel pinches off
- \( I_{ds} \) independent of \( V_{ds} \)
- We say current saturates
- Similar to current source

\[
\begin{align*}
V_{gs} & > V_t \\
V_{gd} & < V_t \\
V_{ds} & > V_{gs} - V_t
\end{align*}
\]
Saturation: $V_{gs} > V_t$ & $V_{gd} < V_t$

Positive Charge on Gate:
Channel exists, Current Flows since $V_{ds} > 0$
But: channel is “pinched off”

$$I_{ds} = (k'/2)(W/L)(V_{gs} - V_t)^2$$
I-V Characteristics

- In Linear region, $I_{ds}$ depends on
  - How much charge is in the channel?
  - How fast is the charge moving?
MOS Transistors – Regions Transitions

FIG 2.2 MOS structure demonstrating (a) accumulation, (b) depletion, and (c) inversion
Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel

- \( Q_{\text{channel}} = \)

SiO\(_2\) gate oxide (good insulator, \( \varepsilon_{\text{ox}} = 3.9 \))
Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- \( Q_{\text{channel}} = CV \)
- \( C = \)
MOS structure looks like parallel plate capacitor while operating in inversion

- Gate – oxide – channel

\[ Q_{\text{channel}} = CV \]

\[ C = C_g = \varepsilon_{\text{ox}}WL/t_{\text{ox}} = C_{\text{ox}}WL \]

\[ V = \]

\[ C_{\text{ox}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} \]

\[ C_{\text{ox}} = 8.6 \text{fF/um}^2 \]
Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- \( Q_{\text{channel}} = CV \)
- \( C = C_g = \varepsilon_{\text{ox}}WL/t_{\text{ox}} = C_{\text{ox}}WL \)
- \( V = V_{\text{gc}} - V_t = (V_{\text{gs}} - V_{\text{ds}}/2) - V_t \)

Diagram of MOS structure:
- SiO\(_2\) gate oxide (good insulator, \( \varepsilon_{\text{ox}} = 3.9 \))
- Polysilicon gate
- n+ p-type body
- Source - channel - Drain
- Gate voltage (\( V_g \))
- Source voltage (\( V_s \))
- Drain voltage (\( V_d \))
Carrier velocity

- Charge is carried by e-
- Carrier velocity $v$ proportional to lateral E-field between source and drain
- $v =$
Carrier velocity

- Charge is carried by e-
- Carrier velocity $v$ proportional to lateral E-field between source and drain
- $v = \mu E$ & $\mu$ called mobility
- $E =$
Charge is carried by e-

Carrier velocity $v$ proportional to lateral E-field between source and drain

$v = \mu E$ \hspace{1cm} $\mu$ called mobility

$E = \frac{V_{ds}}{L}$

Time for carrier to cross channel:

$- t =$
Carrier velocity

- Charge is carried by e-
- Carrier velocity $v$ proportional to lateral E-field between source and drain
- $v = \mu E$ $\mu$ called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t = L / v$
nMOS Linear I-V

- Now we know
  - How much charge $Q_{\text{channel}}$ is in the channel
  - How much time $t$ each carrier takes to cross

$$I_{ds} =$$
Now we know

- How much charge \( Q_{\text{channel}} \) is in the channel
- How much time \( t \) each carrier takes to cross

\[
I_{ds} = \frac{Q_{\text{channel}}}{t}
\]
Now we know

- How much charge \( Q_{\text{channel}} \) is in the channel
- How much time \( t \) each carrier takes to cross

\[
I_{ds} = \frac{Q_{\text{channel}}}{t}
\]

\[
= \mu C_{\text{ox}} \frac{W}{L} \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}
\]

\[
= \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}
\]

\[
\beta = \mu C_{\text{ox}} \frac{W}{L}
\]
Computed Curves

- Linear Resistor
- $V_{gs} = 5\text{v}$
- $V_{gs} = 4.5\text{v}$
- $V_{gs} = 4.0\text{v}$
nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

\[ I_{ds} = \]
nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta \left( V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat}$$
nMOS Saturation I-V

- If \( V_{gd} < V_t \), channel pinches off near drain
  - When \( V_{ds} > V_{dsat} = V_{gs} - V_t \)
- Now drain voltage no longer increases current

\[
I_{ds} = \beta \left( V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat} \\
= \frac{\beta}{2} \left( V_{gs} - V_t \right)^2
\]
Computed Curves

Vgs = 5v
Vgs = 4.5v
Vgs = 4.0v

Linear Resistor
Shockley 1\textsuperscript{st} order transistor models

\[ I_{ds} = \begin{cases} 
0 & V_{gs} < V_t \\
\beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \\
\frac{\beta}{2} \left( V_{gs} - V_t \right)^2 & V_{ds} > V_{dsat}
\end{cases} \]
Example

- We will be using a 0.180 \( \mu \text{m} \) process for your project
  - From TSMC Semiconductor
  - \( t_{\text{ox}} = 40 \text{ Å} \)
  - \( \mu = 180 \text{ cm}^2/\text{V}^*\text{s} \)
  - \( V_t = 0.4 \text{ V} \)

- Plot \( I_{ds} \) vs. \( V_{ds} \)
  - \( V_{gs} = 0, 0.3, \ldots, 1.8 \)
  - Use \( W/L = 4/2 \lambda \)

\[
\beta = \mu C_{\text{ox}} \frac{W}{L} = (180) \left( \frac{3.9 \cdot 8.85 \cdot 10^{-14}}{40 \cdot 10^{-8}} \right) \left( \frac{W}{L} \right) = 155 \frac{W}{L} \mu \text{A/V}^2
\]
pMOS I-V

- All dopings and voltages are inverted for pMOS
- Mobility $\mu_p$ is determined by holes
  - Typically 2-3x lower than that of electrons $\mu_n$
- Thus pMOS must be wider to provide same current
  - Often, assume $\mu_n / \mu_p = 2$

**FIG 2.8** I-V characteristics of ideal pMOS transistor
Current-Voltage Relations
Long-Channel Device

Linear Region: \( V_{DS} \leq V_{GS} - V_T \)

\[
I_D = k'_n \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)
\]

with

\[
k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}} \quad \text{Process Transconductance Parameter}
\]

Saturation Mode: \( V_{DS} \geq V_{GS} - V_T \)

\[
I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})
\]

Cut-off \((V_{GS} - V_T < 0)\) “no current” (not really)
$I_D$ versus $V_{DS}$ short channel device

- Resistive
- Saturation

$V_{DS} = V_{GS} - V_T$

Long Channel

Short Channel
Rabaey’s unified model for manual analysis

\[ I_D = 0 \text{ for } V_{GT} \leq 0 \]

\[ I_D = k' \frac{W}{L} \left( V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) (1 + \lambda V_{DS}) \text{ for } V_{GT} \geq 0 \]

with \( V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}) \),

\[ V_{GT} = V_{GS} - V_T, \]

and \( V_T = V_{T0} + \gamma \left( \sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|} \right) \)
# Transistor Model for Manual Analysis

**Table 3.2** Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

<table>
<thead>
<tr>
<th></th>
<th>$V_{th}$ (V)</th>
<th>$\gamma$ (V$^{0.5}$)</th>
<th>$V_{DSAT}$ (V)</th>
<th>$K'$ (A/V$^2$)</th>
<th>$\lambda$ (V$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.43</td>
<td>0.4</td>
<td>0.63</td>
<td>$115 \times 10^{-6}$</td>
<td>0.06</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>$-30 \times 10^{-6}$</td>
<td>-0.1</td>
</tr>
</tbody>
</table>
Simple Model versus SPICE

\[ V_{DS} = V_{DSAT} \]

- Linear
- Saturated
- Saturated

\[ V_{DSAT} = V_{GT} \]
Even Simpler: The Transistor as a Switch

\[ V_{GS} \geq V_T \]

\[ V_{GS} = V_{DD} \]

\[ I_D \]

\[ V_{DS} \]

\[ R_{0} \]

\[ R_{mid} \]

\[ R_{on} \]

\[ R_{eq} = \frac{1}{2} \left( \frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD} / 2}{I_{DSAT}(1 + \lambda V_{DD} / 2)} \right) \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left( 1 - \frac{5}{6} \lambda V_{DD} \right) \]
The Transistor as a Switch

Table 3.3 Equivalent resistance $R_{eq} (W/L = 1)$ of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide $R_{eq}$ by $W/L$.

<table>
<thead>
<tr>
<th>$V_{DD}$ (V)</th>
<th>1</th>
<th>1.5</th>
<th>2</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS (kΩ)</td>
<td>35</td>
<td>19</td>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>PMOS (kΩ)</td>
<td>115</td>
<td>55</td>
<td>38</td>
<td>31</td>
</tr>
</tbody>
</table>

This week’s Lab – find $R_{eq}$ for our TSMC 180nm process
Saturation Effects

Discharge of 1pF capacitor, with Vgs of 3, 4, 5 volts. Also, 12k resistor.

Which is the resistor?
More on Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion
Gate Capacitance

- Approximate channel as connected to source
- \( C_{gs} = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL = C_{permicron}W \)
- \( C_{permicron} \) is typically about 2 fF/µm

\[ C_{permicron} \approx 2 \text{ fF/µm} \]
The Gate Capacitance

The gate capacitance is given by the equation:

\[ C_{\text{gate}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} WL \]

Where:
- \( C_{\text{gate}} \) is the gate capacitance.
- \( \varepsilon_{\text{ox}} \) is the permittivity of the oxide.
- \( t_{\text{ox}} \) is the thickness of the oxide.
- \( W \) is the width of the device.
- \( L \) is the length of the device.

The diagram shows the cross section and top view of a MOSFET device with the gate oxide, source, drain, and gate-bulk overlap highlighted.

Polysilicon gate

Source \( n^+ \)

\( x_d \)

\( L_d \)

Drain \( n^+ \)

Gate-bulk overlap

Top view

Gate oxide

Cross section

© Digital Integrated Circuits Devices
Dynamic Behavior of MOS Transistor
Physical visualization of FET capacitances
MOS Capacitances Behavior!

Fig 2.11 Total gate capacitance of an MOS transistor as a function of $V_{ds}$. 

Copyright © 2005 Pearson Addison-Wesley. All rights reserved.
Most important regions in digital design: saturation and cut-off
Measuring the Gate Cap

![Diagram showing a circuit with a voltage $V_{GS}$ and a graph of gate capacitance (F) vs. $V_{GS}$ (V).]
Diffusion Capacitance

- $C_{sb}$, $C_{db}$
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to $C_g$ for contacted diff
  - $\frac{1}{2} C_g$ for uncontacted
  - Varies with process
Diffusion Capacitance

\[ C_{\text{diff}} = C_{\text{bottom}} + C_{\text{sw}} = C_j \times \text{AREA} + C_{jsw} \times \text{PERIMETER} \]
\[ = C_j L_s W + C_{jsw} (2L_s + W) \]
Calculation of the FET junction capacitance

(a) Top view

(b) Geometry
## Capacitances in 0.25 µm CMOS process

### Values for a Typical Device:

<table>
<thead>
<tr>
<th></th>
<th>$C_{ox}$ (fF/µm²)</th>
<th>$C_O$ (fF/µm)</th>
<th>$C_j$ (fF/µm²)</th>
<th>$m_j$</th>
<th>$\phi_b$ (V)</th>
<th>$C_{jsw}$ (fF/µm)</th>
<th>$m_{jsw}$</th>
<th>$\phi_{bsw}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>6</td>
<td>0.31</td>
<td>2</td>
<td>0.5</td>
<td>0.9</td>
<td>0.28</td>
<td>0.44</td>
<td>0.9</td>
</tr>
<tr>
<td>PMOS</td>
<td>6</td>
<td>0.27</td>
<td>1.9</td>
<td>0.48</td>
<td>0.9</td>
<td>0.22</td>
<td>0.32</td>
<td>0.9</td>
</tr>
</tbody>
</table>
Parasitic Resistances

\[ V_{GS,eff} \]

\[ \begin{align*}
  S & \quad G \\
  R_S & \quad R_D \\
  D
\end{align*} \]

Polysilicon gate

Drain contact

Drain
Final construction of the nFET RC model

(a) nFET

(b) Linear model for nFET
Latchup

(a) Origin of latchup

(b) Equivalent circuit
Summary of MOSFET Operating Regions

- **Strong Inversion** $V_{GS} > V_T$
  - Linear (Resistive) $V_{DS} < V_{DSAT}$
  - Saturated (Constant Current) $V_{DS} \geq V_{DSAT}$

- **Weak Inversion (Sub-Threshold)** $V_{GS} \leq V_T$
  - Exponential in $V_{GS}$ with linear $V_{DS}$ dependence
Level 1: Long Channel Equations - Very Simple

Level 2: Physical Model - Includes Velocity Saturation and Threshold Variations

Level 3: Semi-Emperical - Based on curve fitting to measured devices

Level 4 (BSIM): Emperical - Simple and Popular
## Main MOS SPICE Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPICE Model Index</td>
<td>LEVEL</td>
<td>-</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Zero-Bias Threshold Voltage</td>
<td>VT0</td>
<td>VT0</td>
<td>V</td>
<td>0</td>
</tr>
<tr>
<td>Process Transconductance</td>
<td>k'</td>
<td>KP</td>
<td>A/V2</td>
<td>2E-5</td>
</tr>
<tr>
<td>Body-Bias Parameter</td>
<td>ggamma</td>
<td>V0.5</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Channel Modulation</td>
<td>1</td>
<td>LAMBDA</td>
<td>1/V</td>
<td>0</td>
</tr>
<tr>
<td>Oxide Thickness</td>
<td>tox</td>
<td>TOX</td>
<td>m</td>
<td>1E-7</td>
</tr>
<tr>
<td>Lateral Diffusion</td>
<td>xd</td>
<td>LD</td>
<td>m</td>
<td>0</td>
</tr>
<tr>
<td>Metallurgical Junction Depth</td>
<td>xj</td>
<td>XJ</td>
<td>m</td>
<td>0</td>
</tr>
<tr>
<td>Surface Inversion Potential</td>
<td>2</td>
<td>f</td>
<td>f</td>
<td></td>
</tr>
<tr>
<td>Substrate Doping</td>
<td>NA,ND</td>
<td>NSUB</td>
<td>cm-3</td>
<td>0</td>
</tr>
<tr>
<td>Surface State Density</td>
<td>Qss/q</td>
<td>NSS</td>
<td>cm-3</td>
<td>0</td>
</tr>
<tr>
<td>Fast Surface State Density</td>
<td>NFS</td>
<td>cm-3</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Total Channel Charge Coefficient</td>
<td>NEFF</td>
<td>-</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Type of Gate Material</td>
<td>TPG</td>
<td>-</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Surface Mobility</td>
<td>m0</td>
<td>U0</td>
<td>cm2/V-sec</td>
<td>600</td>
</tr>
<tr>
<td>Maximum Drift Velocity</td>
<td>umax</td>
<td>VMAX</td>
<td>m/s</td>
<td>0</td>
</tr>
<tr>
<td>Mobility Critical Field</td>
<td>xcrit</td>
<td>UCRIT</td>
<td>V/cm</td>
<td>1E4</td>
</tr>
<tr>
<td>Critical Field Exponent in Mobility Degradation</td>
<td>UEXP</td>
<td>-</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Transverse Field Exponent (mobility)</td>
<td>UTRA</td>
<td>-</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>
# SPICE Parameters for Parasitics

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source resistance</td>
<td>$R_s$</td>
<td>RS</td>
<td>$\Omega$</td>
<td>0</td>
</tr>
<tr>
<td>Drain resistance</td>
<td>$R_d$</td>
<td>RD</td>
<td>$\Omega$</td>
<td>0</td>
</tr>
<tr>
<td>Sheet resistance (Source/Drain)</td>
<td>$R_o$</td>
<td>RSH</td>
<td>$\Omega/\omega$</td>
<td>0</td>
</tr>
<tr>
<td>Zero Bias Bulk Junction Cap</td>
<td>$C_{j0}$</td>
<td>CJ</td>
<td>F/m$^2$</td>
<td>0</td>
</tr>
<tr>
<td>Bulk Junction Grading Coeff.</td>
<td>$m$</td>
<td>MJ</td>
<td>-</td>
<td>0.5</td>
</tr>
<tr>
<td>Zero Bias Side Wall Junction Cap</td>
<td>$C_{jsw0}$</td>
<td>CJSW</td>
<td>F/m</td>
<td>0</td>
</tr>
<tr>
<td>Side Wall Grading Coeff.</td>
<td>$m_{sw}$</td>
<td>MJSW</td>
<td>-</td>
<td>0.3</td>
</tr>
<tr>
<td>Gate-Bulk Overlap Capacitance</td>
<td>$C_{gbo}$</td>
<td>CGBO</td>
<td>F/m</td>
<td>0</td>
</tr>
<tr>
<td>Gate-Source Overlap Capacitance</td>
<td>$C_{gs0}$</td>
<td>CGSO</td>
<td>F/m</td>
<td>0</td>
</tr>
<tr>
<td>Gate-Drain Overlap Capacitance</td>
<td>$C_{gdo}$</td>
<td>CGDO</td>
<td>F/m</td>
<td>0</td>
</tr>
<tr>
<td>Bulk Junction Leakage Current</td>
<td>$I_s$</td>
<td>IS</td>
<td>A</td>
<td>0</td>
</tr>
<tr>
<td>Bulk Junction Leakage Current Density</td>
<td>$I_s$</td>
<td>JS</td>
<td>A/m$^2$</td>
<td>1E-8</td>
</tr>
<tr>
<td>Bulk Junction Potential</td>
<td>$\phi_0$</td>
<td>PB</td>
<td>V</td>
<td>0.8</td>
</tr>
</tbody>
</table>
### SPICE Transistors Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drawn Length</td>
<td>L</td>
<td>L</td>
<td>m</td>
<td>-</td>
</tr>
<tr>
<td>Effective Width</td>
<td>W</td>
<td>W</td>
<td>m</td>
<td>-</td>
</tr>
<tr>
<td>Source Area</td>
<td>AREA</td>
<td>AS</td>
<td>m²</td>
<td>0</td>
</tr>
<tr>
<td>Drain Area</td>
<td>AREA</td>
<td>AD</td>
<td>m²</td>
<td>0</td>
</tr>
<tr>
<td>Source Perimeter</td>
<td>PERIM</td>
<td>PS</td>
<td>m</td>
<td>0</td>
</tr>
<tr>
<td>Drain Perimeter</td>
<td>PERIM</td>
<td>PD</td>
<td>m</td>
<td>0</td>
</tr>
<tr>
<td>Squares of Source Diffusion</td>
<td></td>
<td>NRS</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Squares of Drain Diffusion</td>
<td></td>
<td>NRD</td>
<td>-</td>
<td>1</td>
</tr>
</tbody>
</table>
Circuit Simulation Model of CMOS Inverter
Pass Transistors

- We have assumed source is grounded
- What if source > 0?
  - e.g. pass transistor passing $V_{DD}$
Pass Transistors

- We have assumed source is grounded
- What if source > 0?
  - e.g. pass transistor passing \( V_{DD} \)
- \( V_g = V_{DD} \)
  - If \( V_s > V_{DD}-V_t \), \( V_{gs} < V_t \)
  - Hence transistor would turn itself off
- nMOS pass transistors pull no higher than \( V_{DD}-V_{tn} \)
  - Called a degraded “1”
  - Approach degraded value slowly (low \( I_{ds} \))
- pMOS pass transistors pull no lower than \( V_{tp} \)
Pass Transistor Ckts
Pass Transistor Ckts

\[ V_s = V_{DD} - V_{tn} \]

\[ V_s = |V_{tp}| \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]

\[ V_{DD} \]
Effective Resistance

- Shockley models have limited value
  - Not accurate enough for modern transistors
  - Too complicated for much hand analysis

- Simplification: treat transistor as resistor
  - Replace $I_{ds}(V_{ds}, V_{gs})$ with effective resistance $R$
    - $I_{ds} = V_{ds}/R$
  - $R$ averaged across switching of digital gate

- Too inaccurate to predict current at any given time
  - But good enough to predict RC delay
RC Delay Model

- Use equivalent circuits for MOS transistors
  - Ideal switch + capacitance and ON resistance
  - Unit nMOS has resistance $R$, capacitance $C$
  - Unit pMOS has resistance $2R$, capacitance $C$
- Capacitance proportional to width
- Resistance inversely proportional to width

3: CMOS Transistor Theory
RC Values

- Capacitance
  - $C = C_g = C_s = C_d = 2 \text{ fF/µm of gate width}$
  - Values similar across many processes

- Resistance
  - $R \approx 6 \text{ KΩ*µm in 0.6µm process}$
  - Improves with shorter channel lengths

- Unit transistors
  - May refer to minimum contacted device ($4/2 \lambda$)
  - Or maybe 1 µm wide device
  - Doesn’t matter as long as you are consistent
Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter
Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter
Estimate the delay of a fanout-of-1 inverter
Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter

\[ d = 6RC \]